

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Anthony SPENCER) Group Art Unit: Unassigned
Application No.: National Stage of) Examiner: Unassigned
PCT/GB2003/004867)
Filed: May 10, 2005)
For: STATE ENGINE FOR DATA)
PROCESSOR)

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97(b)

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith PTO/SB/08A and PTO/SB/08B - Information Disclosure Statement together with any required copies of patents, publications or other information of which Applicants are aware, which Applicants believe may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

A copy of the International Search Report in which these documents were cited is also attached.

This Information Disclosure Statement is submitted before the mailing date of a first Office Action on the merits and therefore no fee is required.

It is requested that the information disclosed herein be made of record in this application.

Respectfully submitted,
POTOMAC PATENT GROUP PLLC

By:



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Date: May 10, 2005

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete if Known	
Application Number	New National Stage 607534
Filing Date	May 10, 2005
First Named Inventor	Anthony SPENCER
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	0120-034

Stage 10/534430

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

**Examiner
Signature** _____ **Date
Considered** _____

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Sheet 2 of 2 Attorney Docket Number 0120-034

Application Number	New National Stage 60/534,430
Filing Date	May 10, 2005
First Named Inventor	Anthony SPENCER
Art Unit	Unassigned
Examiner Name	Unassigned

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	International Search Report of PCT/GB2003/04867 dated February 8, 2005	
	2	Ingersoll, S., et al., "Dataflow computation with intelligent memories emulated on field-programmable gate arrays (FPGAs)," Microprocessors and Microsystems, Vol. 26, No. 6,	
		August 2002, pp. 263-280, Great Britain	
	3	Elliott, D., et al., "Computational RAM: Implementing Processors in Memory," IEEE Design & Test of Computers, IEEE Computers Society,	
		Vol. 16, No. 1, January 1999, pp. 32-41, United States	

Examiner Signature	Date Considered
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